Memec Spartan-II LC Development Board
Hello World Reference Design

July 21, 2003
Version 1.0

Overview

This document describes a simple reference design that uses the Xilinx MicroBlaze™ soft processor core along with the uart peripheral core to provide a simple RS232 interface to the UART device located on the Memec Spartan-IIE LC MicroBlaze™ development board.

Objectives

At the conclusion of this reference design, the user should be able to open and compile an EDK project and download the EDK-produced bitstream to the Spartan-II LC development board.

Experiment Setup

Software

The recommended software setup for this reference design is:

- Windows2000 or WindowsXP
- Xilinx ISE 5.2i Foundation with Service Pack 3 (5.2.03)
- Xilinx EDK 3.2 with Service Pack 2 (3.2.2)

Hardware

The hardware setup used by this reference design includes:

- Computer with a minimum of 128 MB RAM and 128 MB Virtual Memory[1]
- Spartan-II LC Development Kit, including:
  - Spartan-II LC development board
  - AC/DC 5V/2A supply
- DB9M-to-DB9F serial cable
- JTAG Parallel-3 programming cable

Refer to Figure 1 for jumper locations. The Memec Spartan-II LC board should be configured as follows:

1. Remove all three J1 jumpers (FPGA mode select jumpers).
2. Install jumper on J11.
3. Install jumper on J7 (pins 1-2).
4. Make sure a 25 MHz 3.3V oscillator is plugged into socket Y1.
5. Connect the JTAG cable to J2 and the parallel port of the PC.

[1] Reference Xilinx Answer Record 10632 at www.support.xilinx.com

6. Connect a straight through RS232 cable to the board's DB-9 connector (JD1) and the serial port of the PC.
7. Verify the Power switch, SW1, is in the OFF position.
8. Connect the 5V AC/DC adapter to JP1.
9. Slide the power switch to the ON position.
10. Verify that the two LEDs on the lower left hand side of the board are ON (DS1, DS2 → ON).

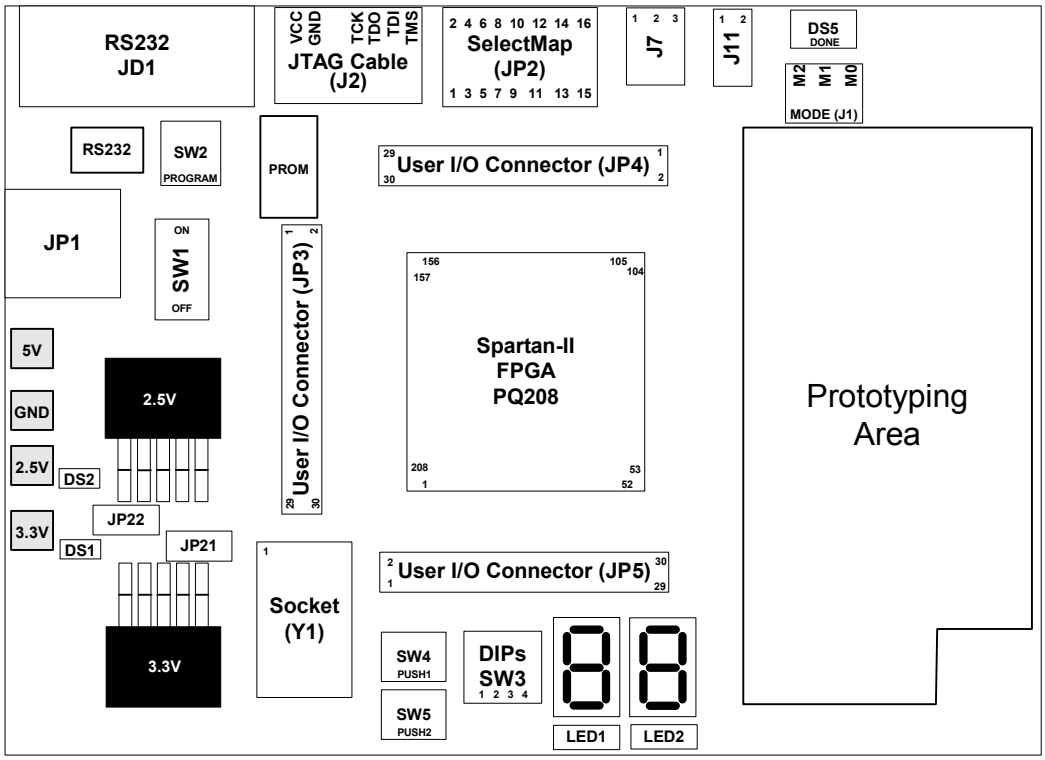


Figure 1 – Memec Spartan-II LC Jumper Locations

Processor System Design

This section discusses the design of the MicroBlaze processor system.

Processor Block Diagram

Figure 2 shows a high-level block diagram for this reference design.

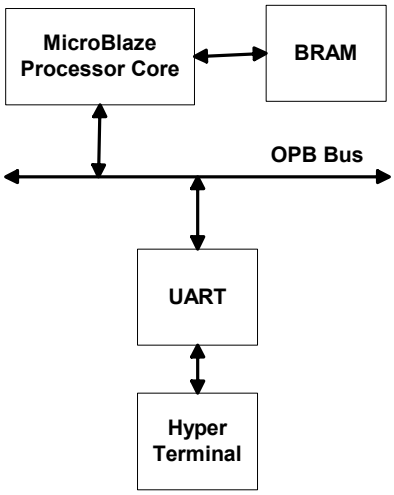


Figure 2 - Hello World Design

Memory Map

The MicroBlaze™ processor provides 4G of address space that can be used to access memory and I/O devices that reside on the processor bus. For this reference design, the UART device located on the MicroBlaze™ development board and the processor memory are memory mapped as shown in Figure 3.

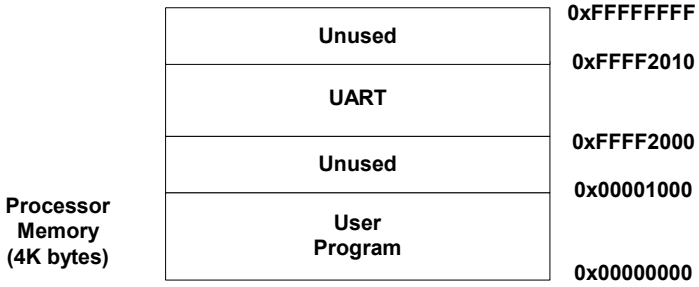


Figure 3 – Processor Design Memory Map

Data and Code Memory

The data and code for this application will reside in the on-chip BlockRAM. The Spartan-II LC development board uses an XC2S100-5PQ208 FPGA, which contains a total of 10 BlockRAMs. This reference design uses 8 BlockRAMs to provide 4K bytes of memory to the processor.

UART Port

The UART port for this reference design is used to interface to the HyperTerminal.

Experiments

Compiling the Project

1. Start Xilinx Platform Studio (XPS) and open a project (**File→Open Project**)
2. Browse to Memec_S2LC_HelloWorld_V1_0\Hello_World_EDK322. Select system.xmp, and select **Open**. XPS should look similar to Figure 4.

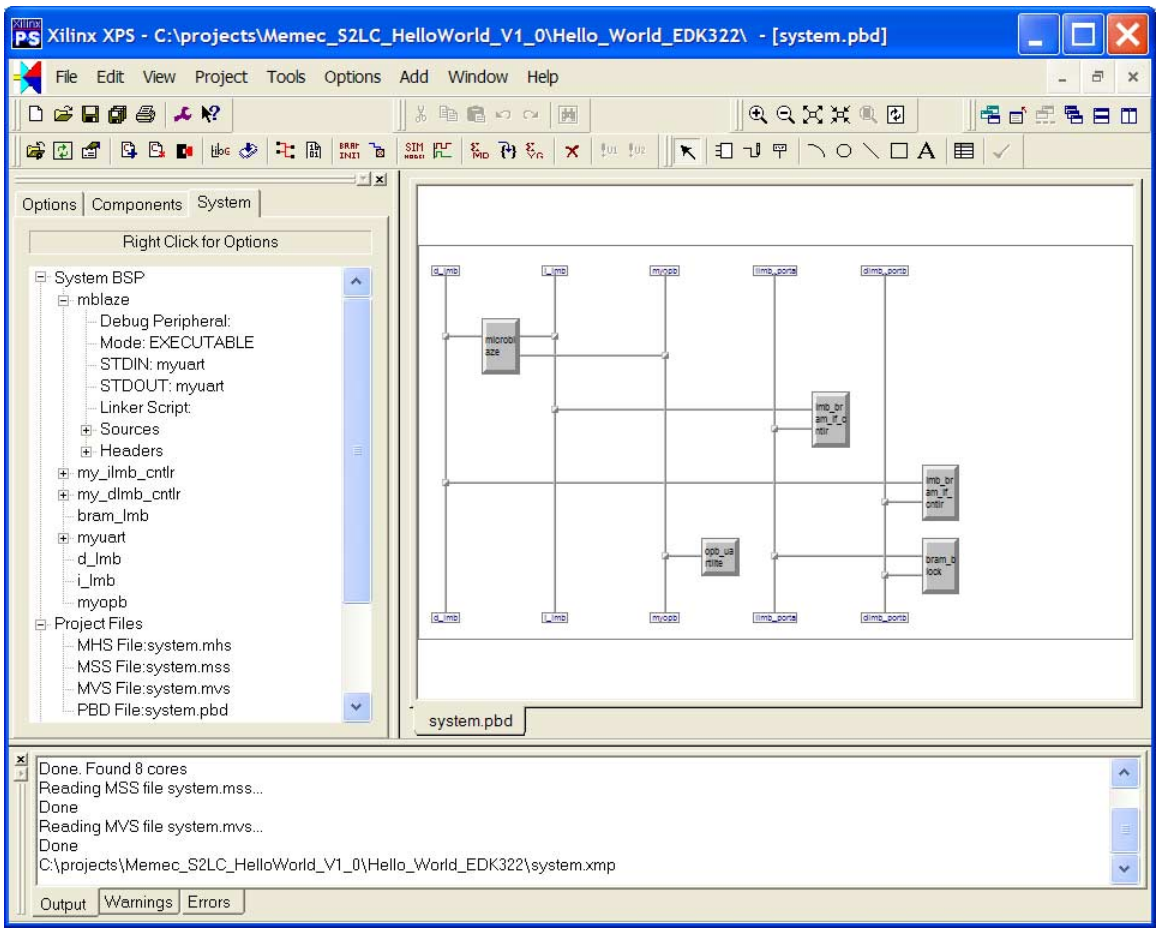


Figure 4 – XPS Hello World Project Opened

3. Generate the software libraries (**Tools→Generate Libraries**)
4. Compile the software program sources (**Tools→Compile Program Sources**)
5. Generate the FPGA hardware netlist (**Tools→Generate Netlist**)
6. Generate the FPGA bitstream (**Tools→Generate Bitstream**)
7. Update the FPGA bitstream with the software program initialized into the on-board BlockRAM (**Tools→Update Bitstream**)

Starting a HyperTerminal Session

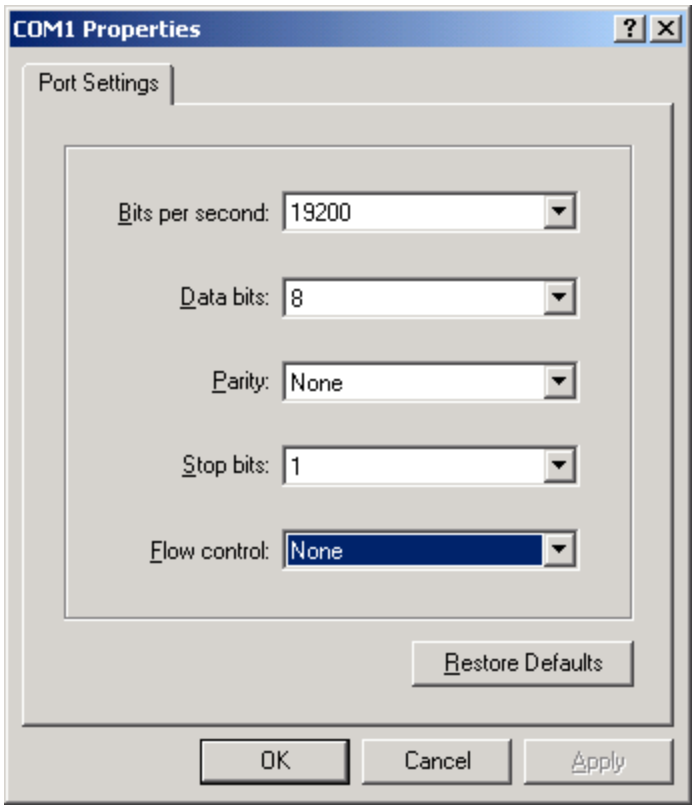
A HyperTerminal will be used to display the UART output from the MicroBlaze. If the serial cable is connected to COM1, the included **com1_19200_8n1n.ht** file can be

double-clicked to launch HyperTerminal. Otherwise, follow the steps below to set up HyperTerminal manually.

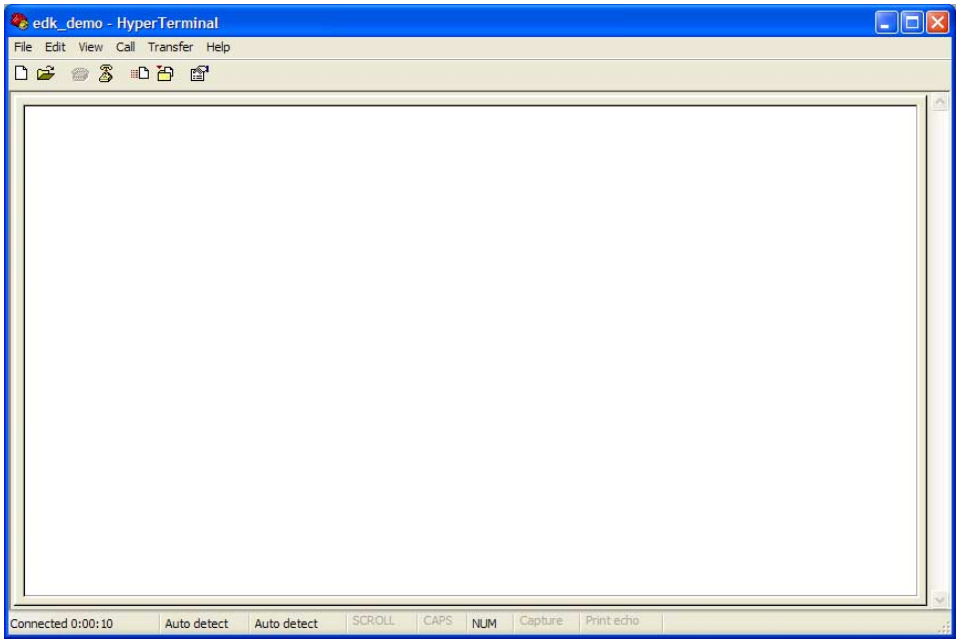
8. Start a HyperTerminal session:
   (Start→Programs→Accessories→Communications→HyperTerminal)

9. Enter edk_demo in the "Name" field and select OK.

10. Select "COM1" from "Connect using" drop down menu and select OK.

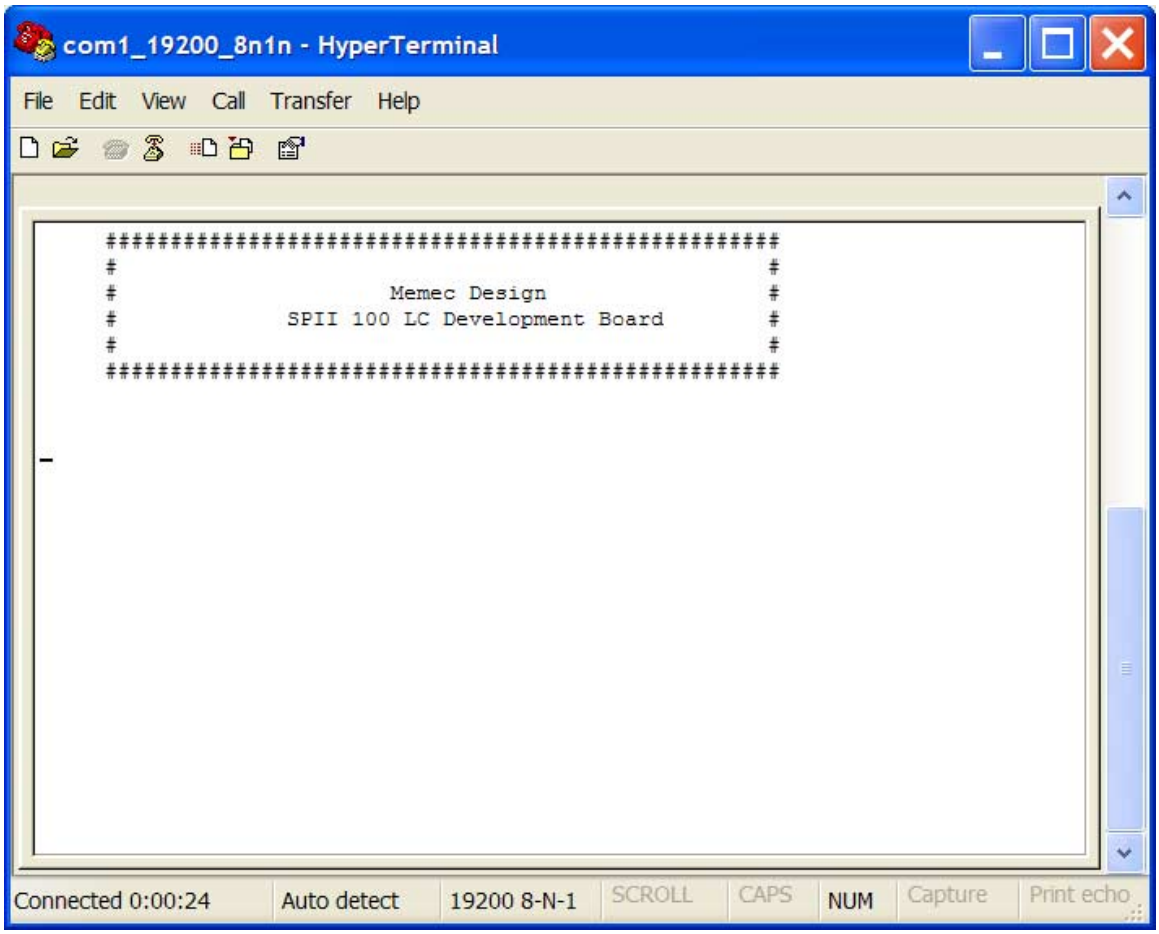


11. Enter the above port settings and then select OK. You should see the following HyperTerminal window.



Running The Application Program

12. Go to the XPS GUI and download the bitstream into the FPGA (**Tools→Download**). Upon completion of the download, you should see the following on the HyperTerminal.



Revision History

Date	Version	Revision
07/21/03	1.0	Initial Memec release.